A 2 GHz High-Gain Differential InGaP HBT Driver Amplifier Matched for High IP3

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Abstract **— A 2GHz single-stage linear InGaP HBT differential driver amplifier is presented operating at I_C = 30mA and V_C = 3V. The amplifier utilizes a collector-base capacitance neutralization technique, yielding a maximum stable gain of 30dB at 2GHz. Furthermore, second-harmonic control is implemented in the in- and output terminations yielding a 20dB reduction of third-order intermodulation distortion (IM3). Moreover, the well-defined second-order terminations result in a good symmetry of the lower and upper IM3 side bands.**

I. Introduction

The market for third-generation (3G) wireless communication systems requires RF building blocks that are highly integrated, linear and efficient. This paper presents two techniques, which provide high gain and low distortion in bipolar differential driver amplifiers.

The first technique is neutralization of the collector-base capacitance (C_{bc}) of a differential common-emitter (DCE) stage by employing bridge neutralization [1], yielding high out-to-input isolation. Consequently, we can achieve a high stable gain, while its unilateral behavior simplifies the matching. Moreover, the higher gain will reduce the amount of amplifier stages or drive-level needed. This is of interest for many applications where high gain is required. Until now, no reports were presented (to the authors knowledge) showing the use of this technique in the RF or microwave regime for large-signal applications.

The second technique is the high-frequency cancellation of third-order intermodulation distortion (IM3) [2]. This technique is based on the cancellation of direct third-order non-linear terms by second-order non-linear terms, originating from the exponential base-emitter junction, when the harmonics at Δf and $2f$ at the in- and the output of the amplifier are properly terminated. As a result, the upper and lower IM3 side bands are eliminated without introducing asymmetry between them [3]. In a differential configuration, these out-of-band signals appear as common-mode (CM) signals, which can be treated separately from the fundamental or differential-mode (DM) signals. Therefore, no trade-off is needed in order to maximize linearity at the expense of gain, which is usually the case when using emitter degeneration [4]. On the contrary, the presented circuit techniques provide orthogonality in the requirements for gain and linearity.

First, Section II reviews the design aspects related to the neutralization of a DCE-stage. Following, Section III explains how the optimum out-of-band terminations for IM3-cancellation are implemented and discusses some theoretical aspects. Finally, Section IV presents the practical implementation of the complete amplifier and summarizes the most important features.

II. Neutralization of a DCE-Stage

Fig. 1 shows the neutralized DCE-stage, in which two collector-depletion capacitances ($Q1_c$ and $Q2_c$) are cross-connected (thus in anti-phase) in order to eliminate the effect of C_{bc} in Q_1 and Q_2.

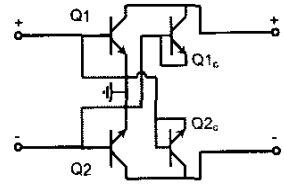

Fig. 1. Neutralization in a differential CE-amplifier using cross-coupled collector depletion capacitors.

The advantage of using on-chip compensation is, that it is bias and temperature independent within the limits of the junction breakdown voltages [1].

Three DCE-stages were fabricated in Triquint's InGaP HBT process (f_T = 28GHz) [5]. In this work we use a transistor with an emitter area of 405μm^2. Fig 2 shows the implementation of a conventional DCE-stage (A), one neutralized with MIM capacitors (B), and one neutralized with collector depletion capacitors ($C_{bc,c}$) (C). The area of

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Q_{1c} and Q_{2c} is made 5% smaller than Q_1 and Q_2, to compensate for the higher off-state $C_{bc,c}$ of Q_{1c} and Q_{2c}. This is important since overcompensation of the DCE-stage can lead to potential instability again.

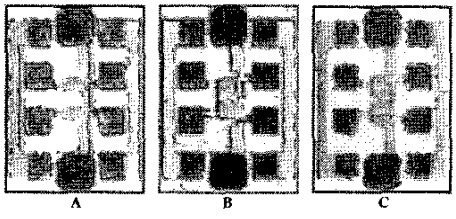

Fig. 2. A conventional DCE-stage (A), a stage neutralized with MIM capacitors (B), and a stage neutralized with collector depletion capacitors (C).

An HP 8753E VNA connected to an ATN4000 4-port test set is used to obtain the differential S_{DM}-parameters. Table I compares the small-signal DM-performance of these stages in terms of the Rollett stability factor (K), the maximum available gain (MAG), the maximum stable gain (MSG), and the isolation. MAG is specified for transistors when K>1, and MSG when K<1 [6]. Table I shows that DCE-stage C is unconditionally stable, independently of the collector voltage (V_C) compared to stage B, which uses linear MIM capacitors. Consequently, DCE-stage C obtains a maximum power gain of 30dB with a simultaneous conjugate match, while a conventional DCE-stage (A) achieves only 21dB with potential instability.

TABLE I
COMPARISON OF THE DCE-STAGES
(I_C = 30mA and f = 2GHz)

DCE stage	V_C [V]	MAG [dB]	MSG [dB]	K	Isolation [dB]
A	2	-	20.5	0.34	23.2
	3	-	21.3	0.37	24.5
	4	-	22.0	0.42	25.7
B	2	-	28.6	0.85	36.5
	3	29.5	-	1.12	41.9
	4	-	30.2	0.44	37.2
C	2	29.8	-	1.08	41.6
	3	30.3	-	1.05	42.2
	4	30.7	-	1.06	42.8

While the above was based on small-signal considerations, we will now apply differential large-signal conditions in order to investigate stability, power-added efficiency (PAE), and maximum output power ($P_{O,max}$) of DCE-stage A and C. It is interesting to verify whether the amplifier remains stable when driven into compression, since the transistors operate at higher current levels and temperatures. For this purpose a load-pull setup is used for differential PA characterization [7]. Fig. 3 shows the gain-contour plots, the optimum differential load impedance for PAE and $P_{O,max}$ ($Z_{L,PAE}$ and $Z_{L,Po}$) plotted in a Smith-chart when DCE-stage C is biased in moderate class-AB operation (I_C = 30mA, V_C = 3V) at 2GHz. Also shown are the power-gain circles, the output-stability circle, and the optimum differential load impedance for power gain ($Z_{L,Gp,max}$), which were calculated from the *S*-parameter data under the same bias conditions. Note that the gain contours were measured at a backed-off power level of P_O = 15dBm.

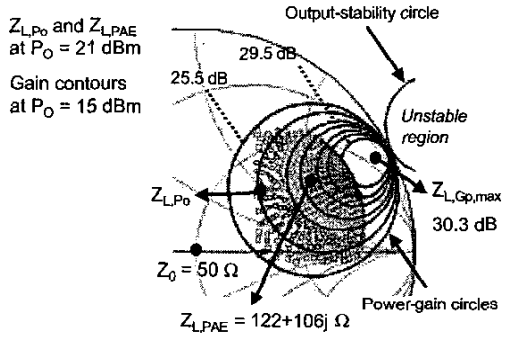

Fig. 3. Large-signal gain-contours (symbols) with the optimum differential loads for PAE, and $P_{O,max}$ together with the small-signal power-gain (lines) and output-stability circle of DCE-stage C at f = 2GHz, I_C = 30mA, and V_C = 3V.

The measured large-signal gain contours shows good agreement with the small-signal power-gain circles, derived from the 4-port *S*-parameter data indicating the accuracy of the differential load-pull calibration [8]. As expected, the unstable load-region is completely outside of the Smith-chart, since K>1. Unfortunately, $Z_{LGp,max}$ could not be applied since we were bounded by the relative high losses (2dB) in the network between the single-ended tuner and the differential output port of the DUT.

Fig 4 shows the transducer power gain (G_T) and PAE versus output power for the DCE-stages A and C when applying $Z_{L,PAE}$, which proved to be the best compromise for gain and output power for both stages.

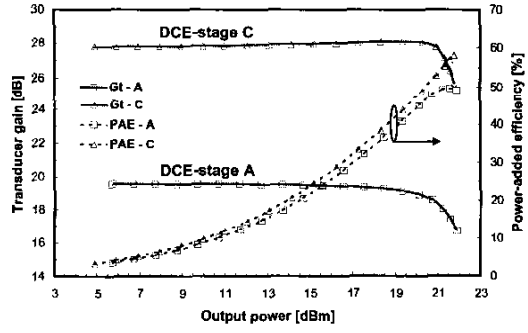

Fig. 4. Measured PAE and G_T versus output power at f = 2GHz, I_C = 30mA, and V_C = 3V for DCE-stage A and C.

The results shown in Fig. 4 prove that a very high and stable gain is obtainable up to compression for C_{bc}-compensated DCE-stages at RF frequencies. The efficiency is 8 percent better at 1dB gain-compression ($P_{O,1dB}$) compared to the normal DCE-stage.

III. IM3 Cancellation in a Neutralized DCE-Stage

A common way to reduce distortion in a CE amplifier is to apply series feedback (or emitter degeneration) [4]. A drawback of this technique is that you also reduce the available gain of the amplifier stage. However, a simultaneous match for gain/power and linearity is possible when controlling the harmonic impedances at $\Delta f = (f_2 - f_1)$ and $2f$ $2f_1$ $2f_2$ in a single-ended or differential configuration [2], [3].

Fig. 5 shows a simplified circuit schematic of the neutralized DCE-stage with common-mode control impedances $Z_{C,S}$ and $Z_{C,L}$ at the in- and output transformers, respectively. Through $Z_{C,S}$ and $Z_{C,L}$, one can set the ratio between the fundamental and second-order components needed at the base-emitter junction to set the condition for cancellation of the resultant IM3, while maintaining symmetry in the lower and upper side bands. In [2] requirements were obtained for high-frequency IM3 cancellation regarding the common-mode impedances at the in- and output transformers. The requirements on $Z_{C,S}$ are given in (1), but this time including the contribution of the compensation capacitors $C_{bc,c}$.

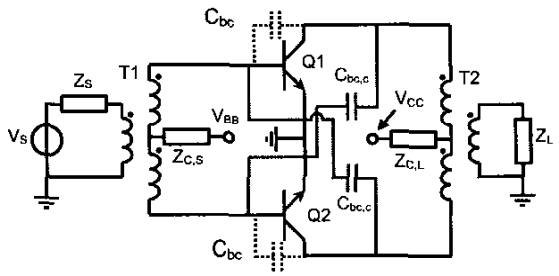

Fig. 5. Neutralization in a DCE-amplifier using cross-connected collector-base depletion capacitors.

$$
\begin{aligned}
Z_{C,S}(\omega) &= 1/\left(G_{C,S} + j\omega C_{C,S}\right) \\
G_{C,S} &= 4g_m/\beta_F \\
C_{C,S} &= 4C_{be,d} - 2(C_{be,t} - C_{bc} - C_{bc,c}) \\
C_{be,d} &= \tau_F g_m
\end{aligned}
\qquad (1)
$$

where τ_F and β_F are the forward transit time and the ideal forward current gain, respectively. Furthermore, $C_{be,d}$, and $C_{be,t}$ are the diffusion and depletion capacitance at the base-emitter junction, respectively. Note, that neutralization of C_{bc} has only effect on DM signals, while feedback of CM signals will still occur via C_{bc} and $C_{bc,c}$. This basically means that the total collector-base capacitance in CM is increased by a factor 2. Therefore, all CM feedback capacitance must be included in $Z_{C,S}$, while $Z_{C,L}$ is a short circuit for the second-harmonic signals at $2\omega_1$, and $2\omega_2$. Note that the requirements presented here are based on an ideal Gummel-Poon model, in which base and emitter series resistances are neglected and all depletion capacitances are assumed to be linear. These requirements have served as initial values in the final amplifier design.

IV. Final Implementation

The final implementation of the amplifier operates in moderate class-AB with a quiescent bias point of 30mA (15mA per transistor) and V_C = 3V. The ideal resistive IM3 cancellation requirement for this current level then becomes:

$$R_{C,S} = \frac{\beta_F}{4g_m} = \frac{75}{4*0.015*40} = 31\Omega \qquad (2)$$

Figs. 6a and 6b show the in- and output matching networks of the amplifier including the proper harmonic terminations. For the design of these networks extensive use has been made of the electromagnetic simulator Momentum in Agilent's ADS.

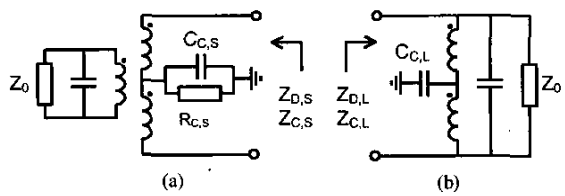

Fig. 6. Input and output differential matching networks including even-harmonic control.

The output matching network is designed to present an optimum differential load impedance $Z_{L,D}$ for gain and efficiency (see Fig. 3). The matching network consists of a differential inductor rather than an output transformer in order to minimize the losses. $Z_{C,L}$ presents a short circuit for $2\omega_1$, and $2\omega_2$ by setting the proper value of $C_{C,L}$ to eliminate the reactive portion of the common-mode inductance for the second-harmonic. The input matching network consists of a transformer which presents a differential source impedance $Z_{D,S}$ in order to conjugately match the input of the amplifier. $C_{C,S}$ sets the proper admittance value of the second-harmonic at the base-emitter junction. $R_{C,S}$ has to be compensated for series resistances in the base, emitter, and any parasitic resistance in the secondary winding of the transformer. Fig. 7 shows the realization of the amplifier. The control resistor $R_{C,S}$ is

not implemented on-chip in order to have more freedom in the experimental verification. The chip was mounted on a Rogers 4003 substrate on which the in- and output bias networks were implemented.

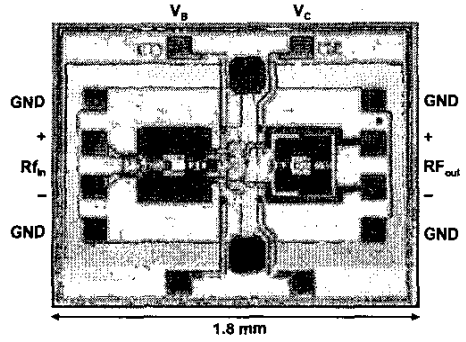

Fig. 7. MMIC realization of the driver amplifier.

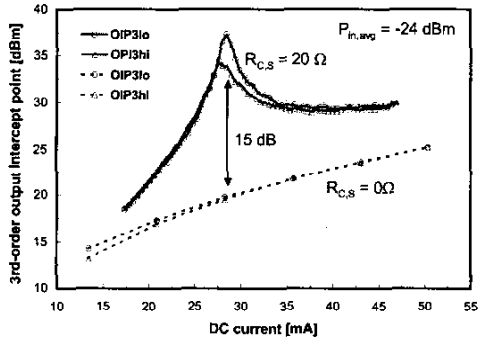

Fig. 8. OIP3 versus DC-current at f = 2GHz with a tone-spacing Δf = 1MHz, and V_C = 3V.

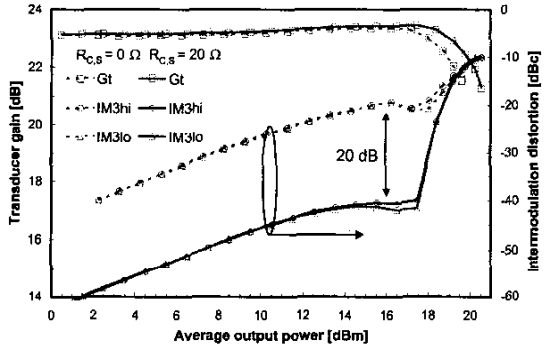

Fig. 9. Gain and IM3 versus output power at f =2GHz with a tone-spacing Δf = 1MHz at I_C = 30mA and V_C = 3V

The required value of $R_{C,S}$ was experimentally determined to be 20Ω, which was as expected lower than the ideal value calculated in (2). Fig. 8 shows OIP3 versus DC-current at f = 2GHz with a tone-spacing of Δf = 1MHz with and without $R_{C,S}$. Fig. 9 shows the two-tone large-signal verification of the amplifier. The results prove that setting the proper second-harmonic impedances yield a 20dB reduction in IM3 versus power up to compression while maintaining good symmetry between the upper and lower side bands (IM3hi and IM3lo). This improvement occurs when biasing the amplifier in a moderate class-AB at 30mA, where we obtain an improvement of up to 15dB in OIP3, measured at an average input power of –24dBm.

V. Conclusion

Neutralization of the collector-base capacitance and IM3-cancellation were combined for the first time in a 2GHz differential InGaP HBT amplifier. The amplifier achieves high stable gain and low IM3 in comparison to a non-compensated differential CE-stage without harmonic control of the baseband and second-harmonic common-mode impedances.

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